

WHAT IS CLAIMED IS:

1. A process for etching a low-k dielectric layer with selectivity to an overlying mask layer, comprising the steps of:

supporting a semiconductor substrate in a chamber of a plasma etch reactor, the semiconductor substrate having a low-k dielectric layer and an overlying mask layer;

supplying an etching gas to the chamber and energizing the etching gas into a plasma state, the etching gas comprising at least one nitrogen reactant, at least one fluorocarbon reactant and optional carrier gas, the fluorocarbon reactant and nitrogen reactant being supplied to the chamber at a flow rates such that the fluorocarbon reactant flow rate is less than the nitrogen reactant flow rate;

etching exposed portions of the organosilicate layer with the plasma so as to etch openings in the low-k dielectric layer with the plasma while providing a etch rate selectivity of the etching rate of the low-k dielectric layer to the etching rate of the mask layer of at least about 5.

2. The process of claim 1, wherein the low-k dielectric layer is above an underlying silicon carbide layer, the etching rate of the low-k dielectric layer being at least 5 times faster than the etching rate of the silicon carbide layer.

3. The process of claim 1, wherein the low-k dielectric layer is above an underlying silicon nitride layer, the etching rate of the low-k dielectric layer being at least 5 times faster than the etching rate of the silicon nitride layer.

4. The process of claim 1, wherein the at least one fluorocarbon reactant is represented by C_nF_m wherein n is at least 4 and m is at least 6.

5. The process of claim 1, wherein the at least one fluorocarbon reactant comprises C_3F_8 , C_4F_8 , C_4F_6 , CF_2H_2 , and mixtures thereof.

6. The process of claim 1, wherein the low-k dielectric layer overlies an electrically conductive or semiconductive layer comprising a metal-containing layer selected from the group consisting of doped and undoped polycrystalline or single crystal silicon, aluminum or alloy thereof, copper or alloy thereof, titanium or alloy thereof, tungsten or alloy thereof, molybdenum or alloy thereof, titanium nitride, titanium silicide, tungsten silicide, cobalt silicide, and molybdenum silicide.

7. The process of claim 1, wherein the openings are 0.25 micron or smaller sized openings.

8. The process of claim 1, wherein the at least one fluorocarbon reactant is a mixture of a hydrogen-free fluorocarbon represented by C_nF_m wherein n is 4 or more and m is 6 or more and a hydrogen-containing fluorocarbon reactant represented by $C_xF_yH_z$ wherein x is 1 or more, y is 1 or more and z is at least 2.

9. The process of claim 1, wherein the etching gas includes a carrier gas selected from the group consisting of Ar, He, Ne, Kr, Xe or mixtures thereof.

10. The process of claim 1, wherein the plasma etch reactor comprises a dual frequency parallel plate plasma reactor having a showerhead electrode and a bottom electrode on which the substrate is supported, the bottom electrode being supplied RF energy at two different frequencies or the showerhead electrode being supplied RF energy at a first frequency and the bottom electrode being supplied RF energy at a second frequency which is greater than the first frequency.

11. The process of claim 1, wherein the flow rate ratio of the fluorocarbon reactant to the nitrogen reactant is 30% or less.

12. The process of claim 1, wherein the fluorocarbon reactant is supplied to the chamber at a flow rate of 3 to 30 sccm and the nitrogen reactant is supplied to the chamber at a flow rate of 50 to 300 sccm.

13. The process of claim 1, further comprising applying an RF bias to the semiconductor substrate during the etching step.

14. The process of claim 1, further comprising filling the openings with metal after the etching step.

APPLIED SEMICONDUCTOR

15. The process of claim 1, wherein the etching step is carried out as part of a process of manufacturing a damascene structure.

16. The process of claim 1, further comprising steps of forming a photoresist layer above the mask layer, patterning the photoresist layer to form a plurality of the openings, etching through the mask, the etching step forming via or contact openings in the low-k dielectric layer at locations where the mask is etched through.

17. The process of claim 1, wherein the openings are formed with an aspect ratio of at least 5:1.

18. The process of claim 1, wherein the etching gas consists essentially of C₅F₈, N₂ and Ar or C₄F₈, CF₂H₂, N₂ and Ar.

19. The process of claim 1, wherein the plasma reactor is at a pressure of 50 to 500 mTorr during the etching step.

20. The process of claim 1, wherein the semiconductor substrate comprises a silicon wafer supported on a substrate support and the substrate support is maintained at a temperature of 20 to 50° C during the etching step.

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